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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/701,035 | 11/03/2003 | Chi-Yuan Hung | 021653-002800US | 6151 |

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| EXAMINER | |
|---|---|
| ROSASCO, STEPHEN D | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 1756 | |

DATE MAILED: 07/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/701,035 | HUNG, CHI-YUAN | |
| | Examiner | Art Unit | |
| | Stephen Rosasco | 1756 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## Detailed Action

The disclosure is objected to because of the following informalities:

page 3, line 18, page 6, line 1, "by each other" should be –from each other-;

page 5, line 16, "that is would";

claim 19, is to a "reticle" but dependent claim 20, recites "The mask of claim 19".

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Yang et al. (6,821,684).

The claimed invention is directed to a mask and a method for manufacturing a mask for integrated circuit devices, the method comprising: providing a mask including a surface region, the surface region including a plurality of spaced regions forming an array configuration, each of the spaced regions being separated from each other by an opaque region to form the array configuration and being characterized by a dimension no greater than 0.25 microns; selectively coding one or more of the spaced regions to define a masked read only memory (ROM) structure, each of the coded spaced regions including a structure, the structure causing an interference with light from a light source; illuminating the

surface region of the mask with the light source to allow the light to traverse through each of the spaced regions, whereupon the selectively coded one or more spaced regions transmits a lower light intensity to a photoresist material than a light intensity on the photoresist material from light illuminated on the photoresist material through the spaced regions free from the one or more codings; and developing the photoresist material to selectively remove portions of the photoresist material only in the portions where light transmitted through the spaced regions free from coding while the portions of the photoresist material corresponding to the one or more coded regions remain intact.

And wherein the structure is selected from a shifter or an anti-scattering bar.

And wherein the one or more coded regions is characterized by a lower transmission rate than a transmission rate of the spaced regions free from coding.

Yang et al. teach a method for fabricating a Mask ROM, comprises: forming a plurality of buried bit lines in a substrate; forming a plurality of word lines and a plurality of first blocking strips thereon on the substrate; forming a plurality of second blocking strips between the word lines and between the first blocking strips; patterning the first blocking strips into a plurality of blocking bumps, wherein the blocking bumps and the second blocking strips together define a plurality of pre-coding windows; forming a coding mask layer having a plurality of coding windows therein on the substrate, wherein the coding windows expose selected pre-coding windows; performing a coding implantation to form a plurality of implanted coding regions under the selected pre-coding windows exposed by the coding windows; and removing the coding mask layer.

And wherein the coding mask layer comprises a patterned photoresist layer.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (6,139,992).

The claimed invention is directed to a mask and a method for manufacturing a mask for integrated circuit devices, the method comprising: providing a mask including a surface region, the surface region including a plurality of spaced regions forming an array configuration, each of the spaced regions being separated from each other by an opaque region to form the array configuration and being characterized by a dimension no greater than 0.25 microns; selectively coding one or more of the spaced regions to define a masked read only memory (ROM) structure, each of the coded spaced regions including a structure, the structure causing an interference with light from a light source; illuminating the surface region of the mask with the light source to allow the light to traverse through each of the spaced regions, whereupon the selectively coded one or more spaced regions transmits a lower light intensity to a photoresist material than a light intensity on the photoresist material from light illuminated on the photoresist material through the spaced regions free from the one or more codings; and developing the photoresist material to selectively remove portions of the photoresist material only in the portions where light transmitted through the spaced regions free from coding while the portions of the photoresist material corresponding to the one or more coded regions remain intact.

And wherein the structure is selected from a shifter or an anti-scattering bar.

And wherein the one or more coded regions is characterized by a lower transmission rate than a transmission rate of the spaced regions free from coding.

Chen et al. teach a photomask, suitable for fabricating a mask-type read only memory (ROM) device, the photomask comprising: a transparent substrate; and

a shielding layer on the transparent substrate, wherein the shielding layer has a pattern layout comprising a code area pattern region and a bonding pad pattern region surrounding the code area region.

wherein the photomask is suitable for a fabrication process, which comprises: providing a semi-manufactured memory device, which comprises a memory region, a bonding pad region, wherein the memory region comprises a plurality of bit lines and a plurality of word lines;

forming a dielectric layer and a barrier layer in sequence on the semi-manufactured memory device;

forming a photoresist layer on the barrier layer;

patterning the photoresist layer with the photomask serving as an etching mask so as to expose a first portion of the barrier layer at the memory region through the code area pattern region and a second portion of the barrier layer at the bonding pad region through the bonding pad region;

etching and removing the exposed first and second portions of the barrier layer simultaneously so that portions of the dielectric layer are exposed by a code area opening and a bonding pad opening; and performing an ion implantation process to code the memory region.

And wherein the photomask comprises a phase shift photomask.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
07/11/05